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Optimized Design of Digital Phase Locked Loops for RF Carrier Acquisition

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Abstract

This paper presents optimized implementation of Digital Phase Locked Loops (DPLL) for generating RF carrier signal used for phase demodulation. The method used for designing DPLL is based on linear control theory and the receiver is phase locked at higher radio frequency signal which is highly noisy. The building blocks of DPLL such as loop filter are implemented with a new method in digital domain for better noise rejection and accuracy. The paper aims to offer aided acquisition of RF signal with fast frequency and phase locking. The designed DPLL is used for higher frequency range applications of the order of GHz and theoretically expected frequency response graph of the filter is verified practically. HDL programming language is used for coding and simulation.

Keywords: DPLL, Loop filter, VCO, Mixer, Phase detector, FPGA, Noise.

Introduction

DPLL finds wide application in areas such as communications, wireless systems, digital circuits and disk drive electronics. DPLL has become possible only in the last thirty years and it is popular for radio frequency electronics today. Noise is an important issue in the field of PLL application and Noise cancellation can be improved by lowering the cut-off frequency of the filter. Since, the input signal considered is a RF signal; this has high noise characteristics and hence designing loop filter and maintaining proper accuracy is also a factor which affects loop dynamics.

There are two distinct modes of phase locked loop behavior i.e., acquisition and tracking. In acquisition mode, PLL is trying to lock onto a signal, in tracking mode PLL is locked onto a signal and will retain that lock through phase and frequency variations of that signal. Acquisition is divided into two types, namely, Self-acquisition and Aided-acquisition. If the loop acquires lock by itself, the process is called Self-acquisition, and if the lock is attained by auxiliary circuits, the process is called Aided-acquisition. In this paper, phase locking is done using auxiliary circuits.

The components such as Phase detector (PD) and Loop filter is designed using VHSIC HDL. HDL is used because of its flexibility for modifying design parameters and to model a digital system.

The paper is divided into several sections as follows: Section II provides the DPLL design and describes the basic building blocks of DPLL. Section III gives Hardware implementation details of DPLL design. Section IV gives the simulation results obtained and finally the last section V provides the conclusion.

DPLL design

Phase locking is a powerful technique that can provide elegant solutions in many applications. DPLL is a negative feedback control system that consists of Phase detector, Loop filter, VCO. DPLL designed consists of analog components such as Mixer, VCO and digital parts such as Phase detector and Loop filter. The basic block diagram of DPLL is shown in Fig.1.

The aim of the paper is to design DPLL for RF carrier acquisition and VCO is to be phase locked to the noisy carrier at the receiver's IF stage to generate a clean local carrier for phase demodulation. The received signal is a Radio frequency signal which is highly noisy in nature. To be called as DPLL, the loop should consist of two properties: 1) output phase is generated in discrete increments 2) error signal generated is a digital number.

A. Building blocks of DPLL

DPLL consists of three important building blocks in order to provide phase locking, namely a

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digital Phase detector, digital Loop filter and an analog VCO. Each block is discussed in detail in this section.

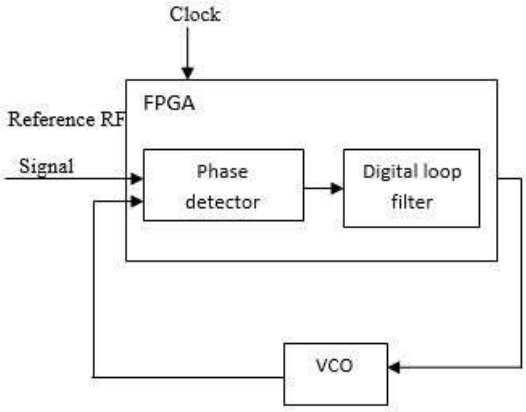

Fig 1: General block diagram of DPLL

1. *Phase detector*

The phase detector block compares the phase of two signals and generates the error signal in terms of frequency and phase between Reference and the VCO. This block is also called as Phase comparator. There are different types of phase detectors, in this paper XOR gate is implemented as PD.

2. *Loop filter*

Loop filter designed is IIR low pass Butterworth filter. It is an important block of DPLL as it affects and determines loop stability. It also provides the necessary control voltage that is required to adjust frequency of VCO. In the design of DPLL, loop filter is the crucial to the operation of the whole phase locked loop. The IIR low pass filter is used to remove unwanted irregularities and is responsible for filtering out the phase error coming out of the phase detector to zero.

The transfer function of the loop filter in Z-domain is given in the equation below

$$H(z) = \frac{b0+b1z^{-1}+b2z^{-2}}{a0+a1z^{-1}+a2z^{-2}} \quad (1)$$

3. *VCO*

Voltage Controlled Oscillator is used for fine adjustment of operating frequency. The output of digital loop filter acts as a control voltage to control oscillation frequency of VCO. The purpose of VCO is to vary an output frequency proportional to control input. As the phase error is increased, the voltage at the VCO input also increases and correspondingly VCO output frequency increases in order to match reference signal.

The transfer function of VCO is given by,

Transfer function = K_{vco} / s (2)

where K_{VCO} =gain of VCO

B. Methodology for implementing Digital Loop filter design

The Fig.2 shows the Digital loop filter which is designed for higher frequency applications such as applications using RF technology.

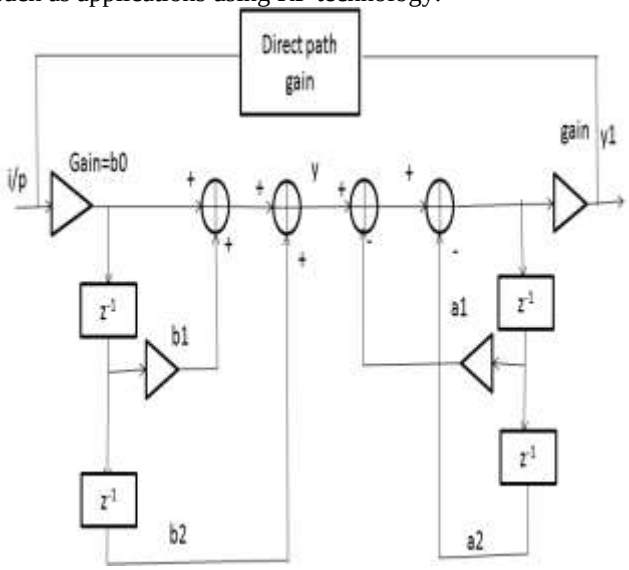

Fig.2: Digital loop filter designed for higher frequency application. H(s) = direct path + integral path (3)

The challenges in designing the above filter is, both the tuning parameters such as direct path gain and low pass filter gain interact with each other and their influence must be controlled appropriately. The low pass filter path acts as an integral term which increases the oscillatory response of the system. Since, both the parameters interact with each other, it can be challenging to arrive at the best tuning values. The theoretical frequency response of the designed filter is shown in Fig.3, where the response of the filter is controlled when it is dropping to zero, this control is due the direct path of the filter. When it comes to ideal low pass filter, the frequency response curve drops to zero, but the designed filter in this paper controls the frequency response and it will make the feedback loop error to approach to some equilibrium point instead of reaching zero.

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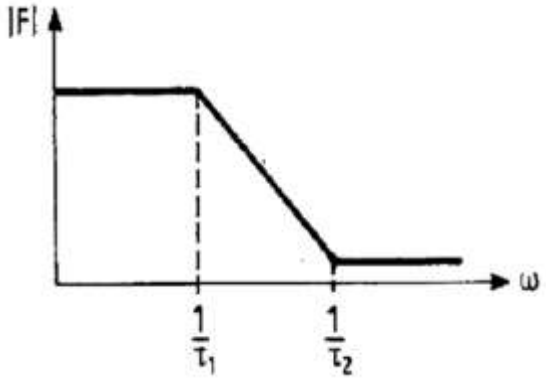

Fig.3: Theoretical frequency response curve for the designed Digital loop filter.

Hardware implementation of dpll design

This section gives the entire structure of hardware implementation of DPLL design. The Fig.4 shows the block diagram of hardware interfacing.

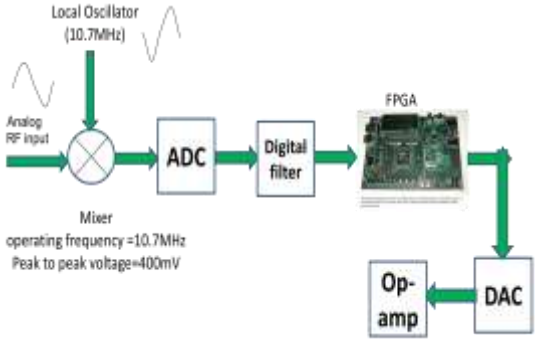

Fig.4: Hardware interfacing structure of DPLL design

The above diagram consists of Mixer which is used for down conversion, ADC for converting analog voltage coming as an output of mixer to digital word, DAC for converting digital output of filter to analog, Op-amp is used because the output of DAC is in terms of current so in order to retrieve voltage this component is used. The inputs to the Mixer is Analog RF input which is of some high frequency value in terms of GHz and Local Oscillators (LO1 AND LO2) are used to down convert high frequency value to low frequency value.

Parameters	DPLL design
Low pass filter gain	1
Sampling frequency	1000 Hz
Cut-off frequency	10 Hz
Direct path gain	2^{-3}

Table I. Design parameters for DPLL

DPLL design simulation results

The simulation results obtained for the DPLL design is described in this section.

A. Phase detector simulation results

The phase detector simulation result is shown in Fig.5 When phase detector detects phase or frequency difference between reference and VCO signal an error is generated. This error is smoothened using Digital loop filter.

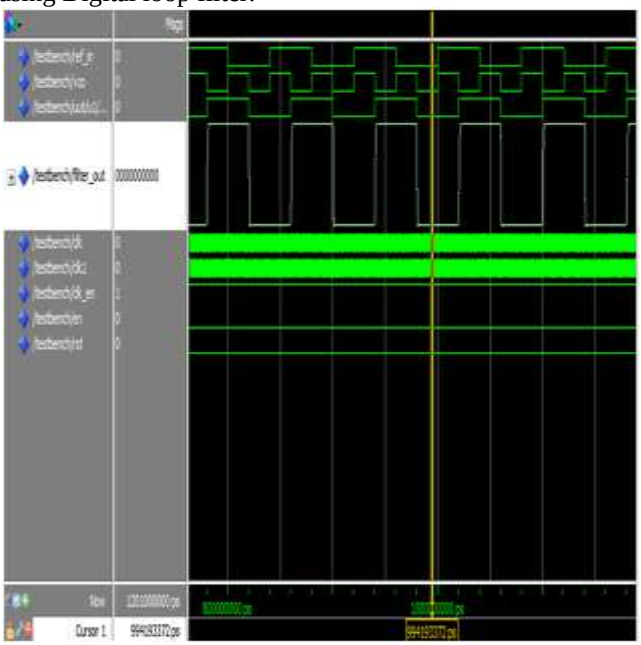

Fig.5: Phase detector and low pass filter simulation results

B. Digital Loop filter simulation results

The loop filter is designed using shift registers, which acts as a delay element. The issues raised during the design of the filter were solved and the result is verified with Microsoft word excel sheet. The Fig. 6 shows the output of Digital loop filter, which consists of Digital word and this output acts as a controlling voltage to VCO. Since the output of Digital loop filter is digital, its output is given to DAC to convert it into analog voltage.

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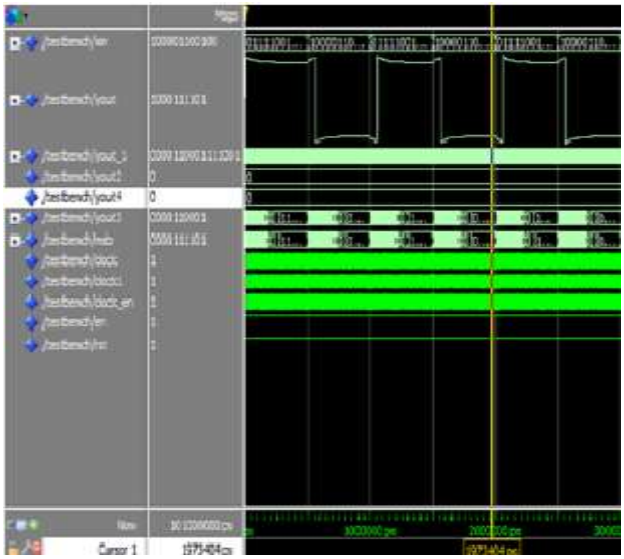

Fig.6: Digital loop filter output in analog format given to DAC

The ADC used is 12 bit and the convention followed by the ADC is shown in Fig.7.

During the design of the filter in VHDL, the ADC convention is considered and correspondingly the digital loop filter is designed. The Fig.8 shows the modification done to the filter input to convert offset binary to two's complement.

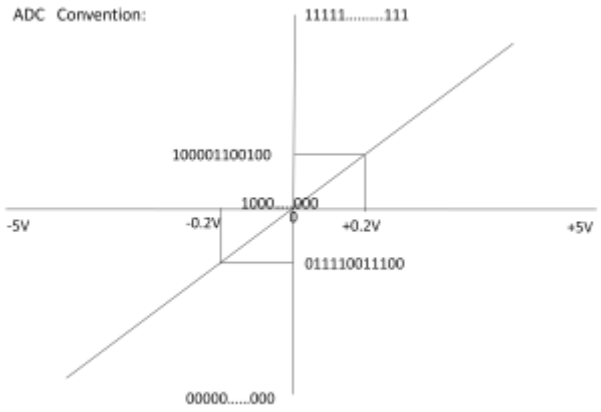

Fig.7 ADC convention

C. Frequency response curve verified using MATLAB

The Digital loop filter designed using VHDL programming

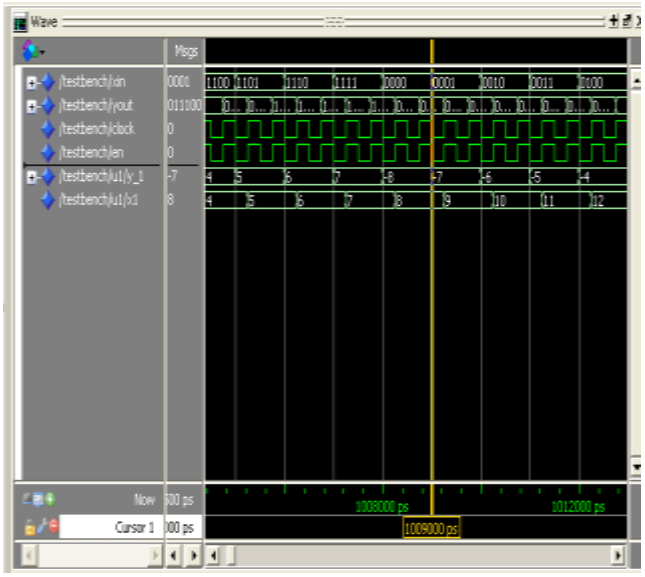

Fig.8 Modification done for the filter input (here it is shown for a 4-bit input)

is tested in MATLAB to examine the required frequency response. The final filter response was matching the required response and it is shown in the Fig.9.

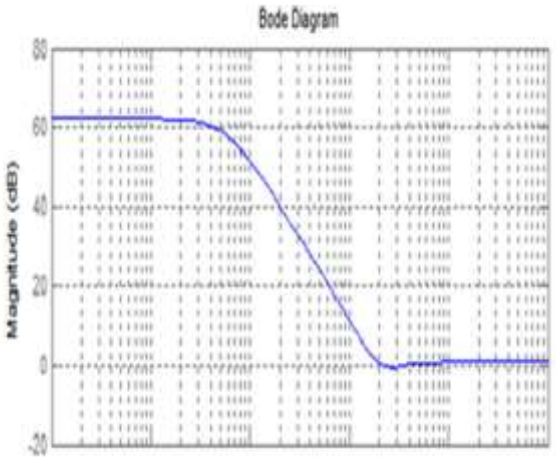

Fig.9: Frequency response of Digital loop filter tested using MATLAB.

Conclusion

This paper aims to design Digital Phase Locked Loop for a RF carrier acquisition in locked condition and it also involves optimized implementation. The implemented loop filter in digital domain was verified for theoretically expected frequency response curve, through simulation results using MATLAB and ModelSim simulator using VHDL programming language. Further, the acquired carrier signal is used for demodulation.

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